IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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| POWER INTEGRATIONS, INC.,<br><br>Plaintiff,<br><br>v.<br><br>FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION,<br><br>Defendants. | ) | **REDACTED PUBLIC VERSION**<br><br><br><br>C.A. No. 04-1371-JJF |

**DECLARATION OF DR. PETER GWOZDZ IN SUPPORT OF DEFENDANTS' MOTION FOR PARTIAL SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,811,075**

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Dated: March 23, 2006

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

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| POWER INTEGRATIONS, INC., a Delaware corporation,<br>Plaintiff,<br>v.<br>FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., a Delaware corporation, and FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,<br>Defendants. | C.A. No. 04-1371<br><br>REDACTED |

**DECLARATION OF DR. PETER GWOZDZ IN SUPPORT OF DEFENDANTS' MOTION FOR PARTIAL SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,811,075**

I, Peter Gwozdz, the undersigned, declare as follows:

1. I have been engaged as an expert by Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. (collectively, "Fairchild") to provide opinions on issues related to U.S. Patent No. 4,811,075. I make this declaration of my own personal knowledge and, if called as a witness, I could and would testify competently to the truth of the matters set forth herein.

2. Attached as Exhibit A is true and correct copy of my Rebuttal Expert Report. This Rebuttal Expert Report accurately sets forth and reflects my opinions.

3. Attached as Exhibit B is a true and correct copy of the tutorial which I attached to my Rebuttal Expert Report. This tutorial accurately sets forth and reflects my opinions.

4. The Colak reference, like the '075 Patent, claims a device structure, not a process for making that structure. Nothing in the Colak reference requires the claimed DMOS structure to be

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5. In 1988 the "DMOS" structure was commonly understood as it is today. Since more than one process was available to form DMOS at that time, one of ordinary skill in the art would not have defined DMOS as requiring successive diffusions through the same opening.

6. The textbook Sze, *Physics of Semiconductor Devices*, Wiley & Sons N.Y. 1981 pp. 431-438, 486-491, describes more than one process for forming a DMOS structure.

7. Attached as Exhibit C is a true and correct copy of "A Novel CMOS-Compatible High-Voltage Transistor Structure", by Zahir Parpia et. Al., IEEE Transactions on Electron Devices, ED-33, Dec. 1986, page 1948 ("Parpia").

8. The issue of determining whether a device is a DMOS device has nothing to do with REDACTED As I stated in my Supplementary Expert Report, ¶¶6-15, the article entitled "A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure", IEDM 83, by H. Wakaumi et. at. ("Wakaumi") discloses a high voltage DMOS device as understood by a person of ordinary skill in the art. Dr. Eklund's notes indicate that he, too, understood REDACTED Importantly, the P body region of the Wakaumi device can be

I declare the foregoing is true and correct under penalty of perjury under the laws of the United States of America.

Executed on March 17, 2006 in Cupertino, California.

Dr. Peter S. Gwozdz

# EXHIBIT A

REDACTED

# EXHIBIT B

REDACTED

# EXHIBIT C

# A Novel CMOS-Compatible High-Voltage Transistor Structure

ZAHIR PARPIA, STUDENT MEMBER, IEEE, JOSÉ G. MENA, STUDENT MEMBER, IEEE, AND C. ANDRE T. SALAMA, SENIOR MEMBER, IEEE

*Abstract*—A novel high-voltage transistor structure, the insulated base transistor (IBT), based on a merged MOS-bipolar concept, is described. This device, which can be implemented using a standard CMOS process, is capable of handling high current densities without latching. The IBT exhibits a fivefold increase in current density compared to the lateral DMOS. A simple technique by which the switching speeds of the IBT can be improved by almost an order of magnitude without significantly compromising its current carrying capability is also presented.

## I. Introduction

A VARIETY of applications in the telecommunications and display areas require high-voltage driver transistors with breakdown voltages in the 100 V range. In these circuits, the high-voltage transistors are generally used only at the outputs, while the rest of the system consists of low-voltage analog or digital control circuits. In order to achieve cost and area savings, the high-voltage transistors must be integrated on the same chip as the low-voltage circuitry. In many such monolithic applications, high-voltage MOS transistors, because of their simplified drive circuitry, are preferred to bipolar transistors. However, the disadvantage of high-voltage MOS transistors is that they offer relatively inferior current handling capabilities as compared to their bipolar counterparts.

The lateral DMOS transistor (LDMOS) is an example of a MOS transistor, suitable for implementation in high-voltage integrated circuits (HVIC's). The cross section of a structure[1] similar to that of the double-diffused MOS transistor and fabricated using a p-well polysilicon gate CMOS process, is shown on Fig. 1(a). The source and the channel region are in the p-well, while a relatively low doped drift (n-substrate) region, (which can be modeled as a resistor $R_D$) separates the $n^+$ drain contact from the channel. The breakdown voltage of the device is determined by the concentration and the length of the drift region. As a general rule, the lower the drift region concentration, the higher is the LDMOS breakdown voltage. However, the low drift region concentrations also mean higher on-resistances. Thus, a trade-off between on-resistance and breakdown voltage exists.

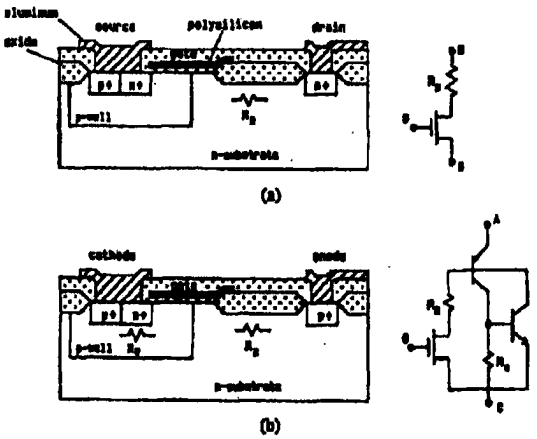


Fig. 1. Device cross sections and equivalent circuits. (a) Lateral DMOS. (b) Lateral IGT.

A structure that combines MOS and bipolar transistors to achieve high current densities, while simultaneously maintaining high input impedance, has recently been proposed. This device, called the insulated gate transistor (IGT) [1], or alternatively the conductivity-modulated FET (COMFET) [2], depends on conductivity modulation of the drift region to dramatically reduce the on-resistance. Lateral IGT (LIGT) structures, proposed and analyzed by various authors [3]–[7], show similar improvements in the on-resistance. A cross section of a LIGT, fabricated using a standard CMOS process, is shown on Fig. 1(b). The LIGT has virtually the same structure as the LDMOS, except that the $n^+$ drain in the LDMOS has been replaced by a $p^+$ diffusion. As its equivalent circuit shows, the LIGT can be modeled as a MOS-gated SCR. During normal operation, the n-p-n transistor is off, and the circuit reduces to that of a MOS-gated p-n-p transistor. However, if the current flowing through the shunt resistor $R_W$ is large enough, the n-p-n will turn on and the LIGT will latch up and gate control will be lost. Another shortcoming of the LIGT is that it has slower turn-off times [4] than the LDMOS because

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IEEE Log Number 8610815.

[1]This structure is not fabricated using the conventional double diffused process but will still be designated as an LDMOS in this paper.

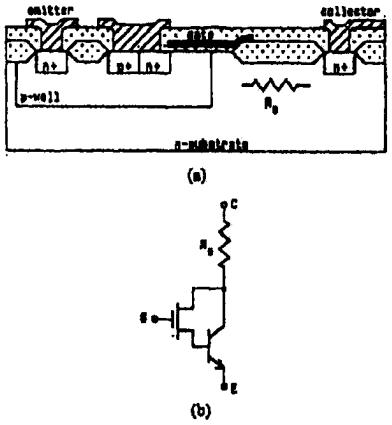


Fig. 2. The insulated base transistor. (a) Device cross section. (b) Equivalent circuit.

the excess carriers in the base of the p-n-p can only be removed through recombination.

In this paper, a novel high-voltage power transistor, that can be easily integrated with low-voltage CMOS circuitry is described. The device is based on a merged MOS-bipolar concept, with the bipolar base current controlled by a MOS gate, hence the acronym IBT (insulated base transistor). The IBT is capable of operating at high current densities, and in contrast to the IGT is latchup free. A simple technique to reduce the turn-off times in the IBT as well improve its breakdown voltage, without significantly compromising its current carrying capability, is also presented. Because this device can be fabricated using a standard CMOS process, high-density analog/digital circuitry as well as high-voltage drivers can be implemented on the same chip.

## II. IBT Structure and Operation

A cross section of the IBT is shown on Fig. 2(a). The device uses a similar structure to that of the LDMOS, with the exception that an extra $n^+$ diffusion is added inside the p-well. This diffusion forms the emitter of a vertical n-p-n bipolar transistor. The p-well and the n-substrate form the respective base and collector of this transistor. The circuit model of the IBT is shown in Fig. 2(b). In this figure, $R_D$ is the drift region resistance.

In normal operation, the collector terminal $C$ is held at a higher voltage than the emitter $E$ and the device current is controlled by the voltage at the gate terminal $G$. In order for the IBT to conduct current, both the MOS and the bipolar transistors must turn on. In the case of the MOS transistor, its gate-to-source voltage has to exceed its threshold voltage $V_{TM}$ while for the n-p-n transistor, its base–emitter junction must be forward biased. Thus the effective turn-on voltage of the IBT is given by

$$V_T = V_{TM} + V_{BE(on)} \tag{1}$$

where $V_{BE(on)}$ is the turn-on voltage of the n-p-n base–emitter junction.

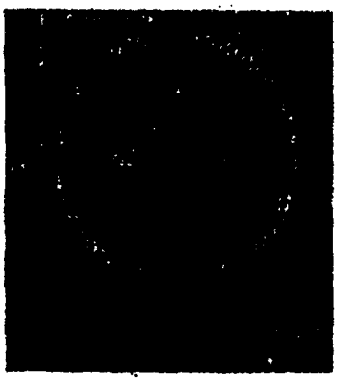

Fig. 3. Photomicrograph of the IBT.

When the gate to emitter voltage $V_{GE}$ is greater than $V_T$, the MOS starts conducting current. This current forms the base current of the bipolar transistor, which in turn is amplified and the resulting collector current $I_C$ is given by

$$I_C = (\beta + 1)I_{MOS} \tag{2}$$

where $I_{MOS}$ is the MOS current at a given gate voltage and $\beta$ is the common emitter current gain of the n-p-n transistor. Thus, assuming $V_{GE} >> V_{BE(on)}$, the IBT will conduct $(\beta + 1)$ times the current of a comparable LDMOS.

## III. Experimental Results

In order to compare device characteristics, LDMOS, LIGT, and IBT high-voltage structures were fabricated using a 5-$\mu$m analog/digital CMOS process.[2] Since no process changes are required to implement the high-voltage devices, the performance of the low-voltage CMOS devices is not affected.

The MOS transistors inherent in all three structures were implemented using identical channel lengths, channel widths, and drift regions. As the photomicrograph of the IBT in Fig. 3 shows, the devices use a circular enclosed collector structure. In order to avoid premature punch-through breakdown in the MOS transistor, a 15-$\mu$m channel length was used. The effective channel width was 750 $\mu$m. The drift region length (length of the n-substrate underneath the field oxide), was 24 $\mu$m. Because of the extra $n^+$ diffusion, the IBT requires approximately 30 percent more area than the LDMOS.

The threshold voltages of the LDMOS and the LIGT are identical to that of the low-voltage n-channel transistors ($\sim$1 V) because they are all fabricated in the same p-well. The IBT has a turn-on voltage of 1.5 V. The I–V characteristics of the IBT are shown on Fig. 4. These exhibit an offset from the origin, which is necessary to for-

[2]In this process, devices are fabricated on a 5-$\Omega$ · cm n-type substrate. An implanted p-well is used for the fabrication of the low-voltage n-channel transistors. Isolation between devices is provided by a 1-$\mu$m LOCOS field oxide. The process uses 850-Å gate oxides and $n^+$ polysilicon gates. The magnitude of the threshold voltage for both the n- and p-channel transistors is 1 V.

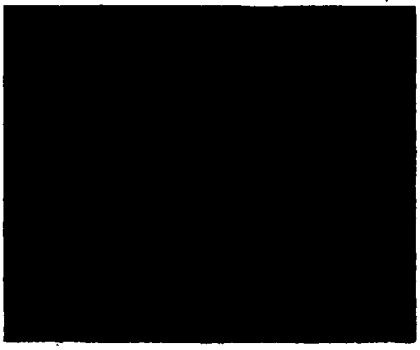

Fig. 4. *I-V* characteristics of the IBT.

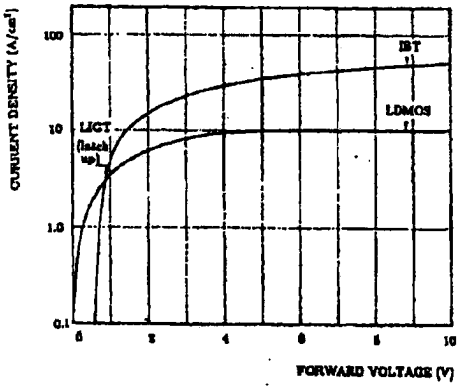


Fig. 5. Forward conduction characteristics of the IBT, LDMOS, and LIGT.

ward bias the bipolar base–emitter junction, and is inherent in all merged MOS-bipolar devices.

The forward conduction characteristics of the three devices, biased at gate voltages of 5 V, are shown on Fig. 5. The current density is calculated by dividing the current in each device by the active device area [4]. For forward voltages exceeding 0.7 V, the IBT exhibits superior current handling capabilities than the LDMOS. In fact, at a forward voltage of 10 V, the IBT exhibits a fivefold increase in current density as compared to the LDMOS.

At low anode currents, the LIGT shows similar forward conduction characteristics to the IBT. However, at anode current densities higher than 4 A/cm$^2$ (in this case, at a current of 2.9 mA), the LIGT latches up. In contrast to the LIGT, neither the IBT nor the LDMOS latch up. The very low value of the LIGT latching current is primarily due to the high sheet resistance of the p-well in this process. Because high-resistivity wells are common to most CMOS processes, the LIGT is not attractive in CMOS-based HVIC's.

The breakdown voltages of the IBT and the LIGT are limited by the common emitter breakdown voltage of the bipolar transistors ($BV_{CEO}$). Thus, they are expected to have lower breakdown voltages than the LDMOS transistor. In this case, while the LDMOS breaks down at 190 V, the LIGT breakdown voltage is 80 V and the IBT breakdown voltages is 70 V.

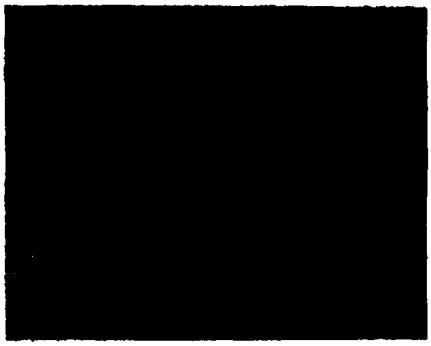

Fig. 6. Transient response of the IBT (2 μs/div horizontal). Curve (*a*) Gate input (5 V/div vertical). Curve (*b*) IBT collector current (20 mA/div vertical). Curve (*c*) Collector current of the improved IBT (20 mA/div vertical).

The switching characteristics of the IBT were investigated under pulsed gate voltage operation. The output current of the device in response to a square wave gate voltage pulse is shown on Fig. 6(b). While the turn-on time of the IBT is relatively short (in the order of 200 ns), it suffers (in common with the LIGT) from long turn-off times. In this case, the 90- to 10-percent turn-off time is approximately 2.2 μs. By comparison, the LDMOS had turn-on and turn-off times of 180 ns. The turn-off transient of the IBT is composed of two stages. The first is an initial fast drop followed by a slow exponential drop. This phenomenon is similar to that observed in the IGT, and has been analyzed by Kuo *et al.* [8]. The fast drop results from the cutoff of the MOS current. After the MOS channel disappears, the n-p-n transistor undergoes open-base turn-off, with the collector current dropping exponentially with time, as the excess carriers in the base decay through recombination. Recombination lifetime control by electron irradiation or heavy metal doping can be used to reduce the fall times. These techniques, however, cannot be applied to the IBT because they can lead to irreparable damage to the low-voltage transistors fabricated on the same chip.

## IV. An Improved IBT Structure

A simple technique to improve the turn-off time of the IBT can easily be implemented. It does not require additional processing steps and consists of reducing the effective carrier lifetime in the base of the bipolar transistor (when the MOS is turned off). This is achieved by placing a shunt resistor $R$ between the bipolar base and emitter, as shown in Fig. 7. Because the bipolar base in the IBT is easily accessible and is also a low-voltage node, a p-well resistor shown in Fig. 7(b) can be used. Since relatively low values of $R$ are required, this resistor can be fabricated adjacent to the IBT without significantly in-

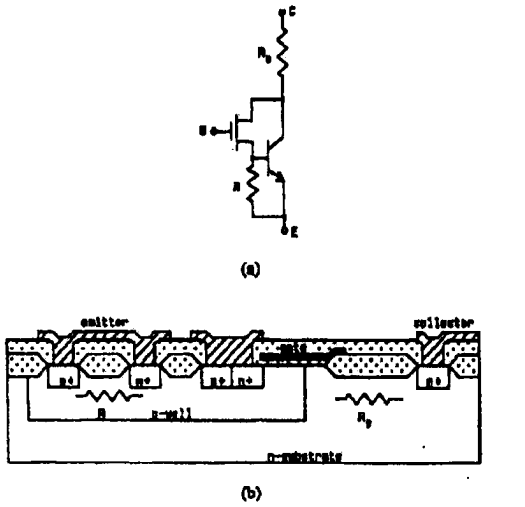


Fig. 7. Improved IBT structure. (a) Equivalent circuit. (b) Device cross section.

creasing the device area. For example, a 500-Ω resistor requires less than 1 percent of the IBT active area.

One drawback of this technique is that it reduces the current-carrying capability of the overall device, since the shunt resistor $R$ lowers the effective current gain of the composite transistor (consisting of the bipolar transistor and the shunt resistor) [9]. Therefore, high-speed operation is achieved at the expense of decreased current density. The IBT current, in the absence of the resistor, is given by (2). Adding resistor $R$, the overall current becomes

$$I_C = (\beta + 1)I_{MOS} - \frac{\beta V_{BE}}{R} \tag{3}$$

where $V_{BE}$ is the base–emitter voltage of the n-p-n transistor.

The turn-off time of the IBT can be analyzed using the equivalent circuit of Fig. 8. This circuit, which models the base–emitter junction of the bipolar transistor by a parallel resistor–capacitor combination, can be used to model the charge in the base region during turn-off. The differential equation describing the relation between $V_{BE}$ and the base current $I_B$ is

$$C_\pi \frac{dV_{BE}}{dt} + \frac{V_{BE}}{R_\pi \| R} = I_B(t) \tag{4}$$

where $R_\pi$ and $C_\pi$ are the respective input resistance and base-charging capacitance of the n-p-n transistor. While both $R_\pi$ and $C_\pi$ are a function of $V_{BE}$, they will be assumed constant in order to simplify the following analysis. Defining the base charge $Q_B = C_\pi V_{BE}$ and $\tau = C_\pi(R_\pi \| R)$, (4) can be rewritten as

$$\frac{dQ_B}{dt} + \frac{Q_B}{\tau} = I_B(t). \tag{5}$$

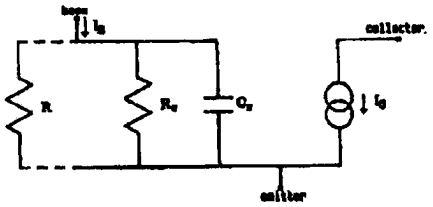


Fig. 8. Circuit used to model the IBT turn-off.

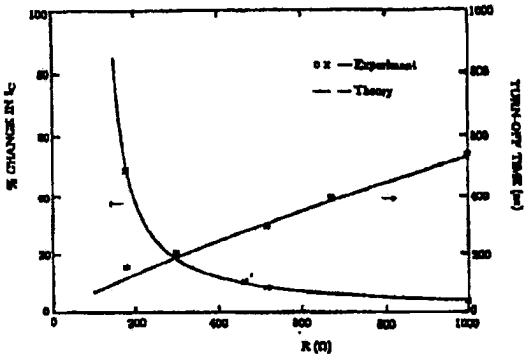


Fig. 9. Change in the collector current and the turn-off time as a function of the shunt resistor $R$.

When the MOS transistor is turned off, $I_B = 0$ and $Q_B(t)$ can be obtained from (5) as

$$Q_B(t) = Q_B(0)e^{-t/\tau} \tag{6}$$

where $\tau$ is assumed constant and $Q_B(0)$ is the base charge right after the initial fast drop. The effect of $R$ is to reduce the time constant $\tau$, resulting in a faster discharge of the base region.

By setting $R_\pi C_\pi = \beta\tau_B$, where $\tau_B$ is the base transit time, the above expression for the base charge $Q_B(t)$ reduces to that developed by Kuo *et al.* [8] for the case where $R = \infty$. The time constant $\tau$ can then be expressed as

$$\tau(R) = \frac{R}{R + R_\pi} R_\pi C_\pi = \frac{R}{R + R_\pi} \beta\tau_B. \tag{7}$$

The total device current $I_C$ can be expressed as [8]

$$I_C(t) = \frac{Q_B(t)}{\tau_B} = I_C(0)e^{-t/\tau} \tag{8}$$

where $I_C(0)$ is the collector current right after the initial fast drop. Using (7) and (8), the 90–10-percent current turn-off time $t_f$ can be written as

$$t_f = 2.2 \frac{R}{R + R_\pi} \beta\tau_B. \tag{9}$$

The concept of adding $R$ to reduce the turn-off time was applied to the fabricated IBT's. The percentage change in the collector current and the turn-off time, as a function of $R$, are shown on Fig. 9. Note that the device current

and the turn off times are as predicted in (3) and (9). The improvement in the turn-off times is significant; for example, for $R = 500\ \Omega$, the fall time is reduced by almost an order of magnitude, at the expense of only an 8-percent decrease in device current. The transient response of the improved IBT, with a 500-Ω shunt resistor is shown in Fig. 6(c). In this case, the turn-off time is reduced from 2.2 μs to 300 ns, while the turn-on time is virtually unchanged. Another advantage of the shunt resistor is that it improves the $BV_{CEO}$ breakdown of the bipolar transistor. In the case of the 500-Ω resistor, the IBT breakdown more than doubles from 70 to 160 V.

## V. Conclusions

A novel high-voltage transistor structure, the insulated base transistor (IBT), was proposed and implemented. The device, which was fabricated using a standard CMOS process, offers higher current densities than comparable LDMOS transistors and better reliability than comparable LIGT's because of its latchup-proof structure. One other advantage of the IBT is that the bipolar transistor and the LDMOS parameters can be varied independently of each other, thus the IBT current density can be further improved by optimizing the design of these transistors. A simple technique for reducing the turn-off time of the IBT, while at the same time increasing it's breakdown voltage, was also demonstrated. This improved IBT structure has breakdown voltages and switching speeds comparable to the LDMOS, while at the same time maintaining high current density operation.

## Acknowledgment

The devices were fabricated under the auspices of the Canadian Microelectronics Corporation.

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**Zahir Parpia** (S'76) was born in Tanzania on December 19, 1959. He received the B.A.Sc. degree in engineering science in 1981 and the M.A.Sc. degree in electrical engineering in 1983, both from the University of Toronto, where he is presently working toward the Ph.D. degree in electrical engineering.

His research interests lie in the general area of semiconductor devices and circuits.

**José G. Mena** (S'84–M'85) received the B.S.E.E. degree in 1975 from the Universidad Central de Venezuela, Caracas, Venezuela, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, Ontario, Canada, in 1981 and 1985, respectively. His Master's research involved the study of power DMOS devices for high-frequency applications, and his doctoral research involved the analysis and optimization of power semiconductor devices.

From 1975 to 1978, he worked at the integrated circuits laboratory of the Venezuelan Institute for Scientific Research (IVIC), Caracas, Venezuela. In 1985, he joined AT&T Bell Laboratories as a Member of Technical Staff. He is currently responsible for the design of smart power IC's. His research interests are in the field of semiconductor power devices and integrated circuits.

**C. Andre T. Salama** (S'60–M'66–SM'84) received the B.A.Sc., M.A.Sc., and Ph.D. degrees, all in electrical engineering, from the University of British Columbia in 1961, 1962, and 1966, respectively.

From 1962 to 1963, he served as a Research Assistant at the University of California, Berkeley. From 1966 to 1967, he was employed at Bell Northern Research, Ottawa, as a Member of Scientific Staff working in the area of integrated circuit design. Since 1967, he has been on the staff of the Department of Electrical Engineering, University of Toronto, where he is currently a Professor. For 1975–1976 he was a Visiting Professor at the Katholieke Universiteit, Leuven, Belgium. He is on the board of directors of the Canadian Microelectronics Corporation (chairman of the Board 1984–1985), a non-profit corporation funded by the Canadian government to further the development of microelectronics design and technology within the Canadian University system in close cooperation with industry and government laboratories. His research interests include the design and fabrication of semiconductor devices and integrated circuits. He has published extensively in technical journals, is the holder of seven patents, and has served as a consultant to the semiconductor industry in Canada and the U.S.

Dr. Salama is a member of the Association of Professional Engineers of Ontario and the Electrochemical Society. He is presently the Chairman of the IEEE Toronto Section.

**CERTIFICATE OF SERVICE**

I hereby certify that on the 23rd day of March, 2006, the attached **REDACTED PUBLIC VERSION OF DECLARATION OF DR. PETER GWOZDZ IN SUPPORT OF DEFENDANTS' MOTION FOR PARTIAL SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,811,075** was served upon the below-named counsel of record at the address and in the manner indicated:

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*/s/ Lauren E. Maguire*

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